#4/IDS 7/18/02 KB

Atty. Dkt. No. 035905-0118

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Igor G. KOUZNETSOV et al.

Title: TWO MASK FLOATING GATE EEPROM AND METHOD OF MAKING

Appl. No.: 10/066,376

Filing Date: 02/05/2002

Examiner: Unassigned

Art Unit: 2823

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), before the mailing date of the first Office Action on the merits.

Atty. Dkt. No. 035905-0118

RELEVANCE OF EACH DOCUMENT

An English translation of the foreign-language documents is not readily available. However, the absence of such translation does not relieve the PTO from its duty to consider the submitted foreign language documents (37 CFR §1.98 and MPEP §609).

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date 6/13/02

By _____

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Attorney for Applicant
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: June 13, 2002

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Sheet	1	of	7

Complete if Known	
Application Number	10/066,376
Filing Date	02/5/2002
First Named Inventor	Igor KOUZNETSOV et al.
Group Art Unit	2821
Examiner Name	Unassigned
Attorney Docket Number	035905-0118

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	B1	4,500,905		Shibata		
	B2	6,185,122		Johnson et al.		
	B3	3,414,892		McCormack et al.	12/13/1968	
	B4	3,432,827		Sarno	3/11/1969	
	B5	4,535,424		Reid		
	B6	4,630,096		Drye		
	B7	4,672,577		Hirose		
	B8	4,710,798		Marcantonio		
	B9	4,811,082		Jacobs		
	B10	5,001,539		Inoue et al.		
	B11	5,089,862		Warner, Jr. et al.		
	B12	5,160,987		Pricer et al.		
	B13	5,191,405		Tomita et al.		
	B14	5,202,754		Bertin et al.		
	B15	5,266,912		Kledzik		
	B16	5,283,468		Kondo et al.		
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	B18	5,422,435		Takiar et al.		
	B19	5,426,566		Beilstein, Jr		
	B20	5,434,745		Shokrgozar et al.		
	B21	5,453,952		Okudaira		
	B22	5,455,455		Kurtz et al.		
	B23	5,468,997		Imai et al.		
	B24	5,471,090		Deutsch		
	B25	5,481,133		Hsu		
	B26	5,495,398		Takiar et al.		
	B27	5,502,289		Takiar et al.		
	B28	5,523,622		Harada et al.		
	B29	5,523,628		Williams et al.		
	B30	5,552,963		Burns		
	B31	5,561,622		Bertin et al.		
	B32	5,581,498		Ludwig et al.		
	B33	5,585,675		Knopf		
	B34	6,612,570		Eide et al.		
	B35	5,654,220		Leedy		
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	B38	5,703,747		Voldman et al.		
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	B42	5,915,167		Leedy		

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Attorney Docket Number	035905-0118

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	B60	EPO	0 073 486	A2	Toyama et al.	8-26-1982		
	B61	JP	61-222216		Yohehara	10-2-1986		
	B62	WO	94/26083		Carson et al.	11-10-1994		
	B63	EPO	0 516 866	A1	Bayer et al.	12-9-1992		
	B64	EPO	0 644 548	A2	Bertin	9-2-1994		
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	B69	JP	6-22352		Toshiba			
	B70	EPO	0 387 834	A2	Wada	9-14-1990		

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
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	B75	DE GRAAF C. et al.: "A Novel High-Density, Low-Cost Diode Programmable Read Only Memory," IEDM, beginning at page 189	
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	B83	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuity".	
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	B93	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEDM, 1996, pgs. 121 - 124.	
	B94	KUROKAWA TAKAKAZU: "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction", FGCS - Future, Generation, Computer, Systems", Vol. 4, No. 2, 1988, pgs. 145-155, Amsterdam, The Netherlands.	

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	B119	Patent Application, AKRAM, US 2002/0030262 A1.	
	B120	Patent Application, AKRAM, US 2002/0030263 A1.	
	B121	Patent Application, LEEDY, US 2001/0033030 A1.	
	B122	Chan et al. "Three Dimensional CMOS integrated Circuits on Large Grain Polysilicon Films" EEE, Hong Kong University of Science and Technology 2000 IEEE	

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